Student's Name

Professor's Name

Course

Date

Lab Report: DC Biasing of an NMOS Transistor

Objective

The experiment aims to study the DC biasing of an NMOS transistor. The study intends to complete a DC analysis of three circuits, including an NMOS biased in the saturation region, one biased in the triode region, and a diode-connected NMOS transistor.

Equipment and Software Listing

Enhancement-type NMOS transistor MC14007

Resistors

Data

Part 1: NMOS in Saturation Mode

The circuit was designed as shown below:

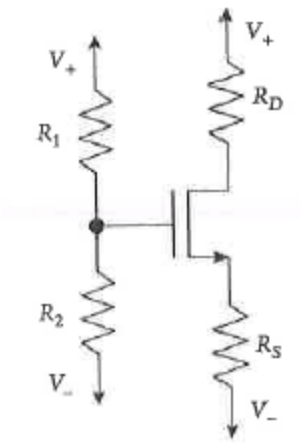

Figure 1: NMOS-biased circuit for saturation

The circuit was designed so that I_D = 1 mA, V_G=*0*V, and V_D = +5 V using supplies of V_+ =-V_- = 15 V.

Part 2: NMOS in Triode Mode

The circuit in figure 1 was redesigned such that I_D = mA, V_D = +2 V and V_{DS} = 0.5 V using supplies of V_+ =-V_- = 15 V and a triode model.

Part 3: Diode-connected NMOS

The circuit was designed as shown below:

Figure 2: Circuit with a diode-connected NMOS transistor

Analysis

In part 1, which involved an NMOS in saturation mode, V_{OV} was calculated based on the specifications of the circuit. The simulation of the circuit gave a datasheet, which was used to find the threshold voltage V_{in} of the transistor. The calculation found V_{GS} to be 15 V. From the datasheet, the range of V_{in} values found among the various sizes of transistors was revealed. The value of V_S was found to be 15 V. Notably, the calculations gave sufficient information, which was used to find R_S to be 0.5 V. The calculated value was available in the kit with slight

deviation. However, it was not possible to find the exact value by combining several resistors because of errors in the experiment. Similarly, the calculations gave sufficient information, which was used to find R_D to be 10 V. The calculated value was available in the kit with slight deviation and it was not possible to find the exact value by combining several resistors because of errors in the experiment. Therefore, the values for R_1 to R_2 that should be used are 10 and 11 V respectively, with the problem lacking specification.

In part 2, which involved an NMOS in triode mode, V_{OV} and V_{GS} were calculated based on the specifications of the circuit. The value of V_G was found to be 0 V. At this point, the information gathered was enough to find R_S, which was 0.5 V and falls within the kit. Conversely, the value could not be achieved by combining several transistors due to errors. In addition, R_D was calculated using the available information and was found to be 10 V and within the kit. Conversely, the value could not be achieved by combining several transistors due to errors. Therefore, the suitable values for R_1 to R_2 that should be used are 10 and 11 V respectively, with the problem lacking specification.

The analysis of circuits in a laboratory setting and their findings are not likely to agree with theoretical values because of numerous sources of error, which compromise the results. One source of error is instrumental errors, which are usually inevitable. The measuring instruments used in the laboratory are designed with inevitable errors, which theoretical values ignore. The errors may be significant and cause slight deviations in experimental results. For example, the resistances of the resistors used in the circuit are not accurate due to design flaws. In addition, errors could emerge from inaccurate power sources, with the voltage varying constantly during

the tests. The wires used to connect the components of the circuit also contribute to resistance, which compromises the findings.

Conclusion

Remarkably, the study and analysis of the DC biasing of an NMOS transistor through the analysis of three circuits including an NMOS biased in the saturation region, one biased in the triode region, and a diode-connected NMOS transistor reveal significant behavior. The analysis of an NMOS biased in the saturation region revealed significant reduction in voltage through the circuit, which supports the objective of the experiment. The analysis of an NMOS biased in the triode region and a diode-connected NMOS transistor proved the effect of transistors on the circuit by dividing the circuit voltage into equal proportions to enable the examination of the qualitative impact of transistor-to-transistor variations, which helps in the design of transistors with effective current regulation and amplification of input signals for practical applications.